Notice of Allowability	Application No.	Applicant(s)	
	10/824,680	NYGAARD, RICHARD A.	
	Examiner	Art Unit	
	Carol S Tsai	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/26/04*.

2. ☒ The allowed claim(s) is/are *2, now renumbered as 1*.

3. ☒ The drawings filed on *4/15/04 & 7/16/04* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

IN THE ABSTRACT:

"An eye diagram analyzer equips each SUT data and clock signal input channel with individually variable delays in their respective paths. For a range of signal delay of n-many SUT clock cycles, the SUT clock signal delay might be set at about n/2. For each data channel there is specified a point in time relative to an instance of the delayed clock signal (data signal delay) and a voltage threshold. The specified combination (data signal delay, threshold and which channel) is a location on an eye diagram, although the trace may or may not ever go through that location. A counter counts the number of SUT clock cycles used as instances of the reference for the eye diagram, and another counter counts the number of times the specified combination of conditions was met ("hits"). After watching a specified combination for the requisite length of time or number of events, the number of SUT clock cycles involved and the associated number of hits are stored in memory using a data structure indexed by the components of the specified combination (data signal delay, threshold). Next, a new combination of data signal delay and threshold is specified and a measurement taken and recorded in the data structure. The process is

repeated until all possible combinations within a stated range of data signal delay and threshold voltage (using specified resolution/step sizes for delay and voltage) have been investigated. As this process proceeds under the control of firmware within the logic analyzer, other firmware can be examining the data structure and generating a partial eye diagram visible on a display, and that will be complete soon after the measurement itself is finished." has been changed to "An eye diagram analyzer equips each SUT data and clock signal input channel with individually variable delays in their respective paths. For a range of signal delay of n-many SUT clock cycles, the SUT clock signal delay might be set at about n/2. For each data channel there is specified a point in time relative to an instance of the delayed clock signal (data signal delay) and a voltage threshold. The specified combination (data signal delay, threshold and which channel) is a location on an eye diagram, although the trace may or may not ever go through that location.".

Allowable Subject Matter

2. Claim 2 is allowed.

3. The following is an examiner's statement of reasons for allowance:

U. S. Patent No. 5,210,712 to Saito in view of U. S. Patent No. 4,445,192 to Haag et al. are references closest to the claimed invention. Saito in combination with Haag et al. disclose an eye diagram analyzer comprising: a clock signal waveform delay circuit having an input for receiving a clock signal and an output producing a delayed clock signal; a threshold detector having a variable threshold, an input for receiving a data signal to be measured as an eye diagram and having an output producing a logical data signal; a variable data signal waveform delay circuit having an input coupled to receive the logical data signal and an output producing a

delayed logical data signal; a transition detection circuit coupled to the delayed clock signal and to the delayed logical data signal, and having an output producing a transition signal indicative of a transition in the delayed logical data signal occurring during a selected length of time subsequent to a transition in the delayed clock signal; a counter coupled to the transition signal and that counts occurrences thereof; and a memory whose content is organized as a data structure indexed by the difference in delays for the variable clock signal waveform delay circuit and the variable data signal waveform delay circuit, by the variable threshold, and that stores in an indexed location the number of counted occurrences. However, Saito in combination with Haag et al. do not teach an output producing a delayed clock signal that is delayed by a selected first amount and whose transitions in a selected direction serve as a time reference; an output producing a delayed logical data signal whose amount of delay is a swept second amount that can range from less than to more than first amount of delay; an output producing a transition signal indicative of a transition in the delayed logical data signal occurring during a selected length of time subsequent to a transition in the selected direction within the delayed clock signal; and a memory whose content is organized as an eye diagram data structure indexed by the signed difference in the first and second amounts of delay by the variable threshold, and that stores in an indexed location the number of counted occurrences that the data signal occupied the indexed location with an eye diagram; and including all of the other limitations in the respective independent claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dollard discloses a decoding system having a clock recovery system for maintaining the optimum time for sampling a signal.

Schlag et al. disclose a method and a regenerative filter for equalizing an input digital signal being proposed, wherein the received input signals is processed by means of threshold decision elements, multiplexers, and a delay unit, which regenerates a delayed signal for switching the multiplexer, wherein the input signal passes in parallel through at least threshold decision elements and the output signals of the threshold decision elements are connected by at least one multiplexer to the delay unit and the delay unit is comprised of at least two delay stages, whose delayed signals switch the at least one multiplexer .

Kobayashi et al. disclose an automatic amplitude equalizer for compensating an amplitude characteristic of an input signal, wherein a control signal for equalizing an inclination amplitude distortion of an input signal is detected making use of a pair of digital demodulated signals to compensate for the amplitude characteristic of the input signal with a high degree of accuracy and which can be constructed with a reduced circuit scale and at a reduce cost.

Guo discloses an all digital data algorithmic recovery method and apparatus which

operates at jitter greater than 25% and where run length is more than 1000 bits and which uses self calibrated delay elements to phase align a locally generated time ruler reference with the data average transition position to reliably establish the sampling time for retrieving data from an incoming binary sequence at the center of the data eye.

LaRosa et al. disclose a clock recovery circuit employing a method of and apparatus for adjusting the phase of a recovered clock signal.

Marzalek et al. disclose a sampling signal analyzer in which the frequency of an input signal to be measured is initially ascertained, an appropriate sampling frequency is then determined, data needed to reconstruct the wave form of the input signal is acquired, and the input signal wave shape is reconstructed with a calibrated time axis and preferably displayed.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for TC 2800 is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (571) 272-1585 or (571) 272-2800.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 872-9306. This practice

may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai
Patent Examiner
Art Unit 2857

10/29/04